Effects of Design, Structure and Material on Thermal-Mechanical Reliability of Large Array Wafer Level Packages

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6) Array size
7) Solder ball shape
8) PCB design

The simulation results are compared to the experimental test data and failure analysis. The mechanisms in enhancing thermo-mechanical reliability of WLP are discussed.

2. WLP Descriptions

Four different WLP packages, as shown in Table 1, are studied.

2009 International Conference on Electronic Packaging Technology & High Density Packaging (ICEPT-HDP)
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Table 1 WLP descriptions

WLP Structures	Descriptions
WLP Structure A	Standard WLP (Ball on I/O)
WLP Structure B	Ball on polymer without UBM
WLP Structure C	Ball on polymer with UBM
WLP Structure D	Encapsulated copper post

2.1 WLP Structure A: Standard WLP

Ball on I/O WLP is a standard wafer level packaging technology and the process is very similar to a typical flip chip technology. As shown in Figure 1, the ball is attached to the aluminum pad directly through under bump metallurgy (UBM). The bumps are directly attached to the final I/O metal pad. Passivation opening, overlapped by UBM, provides a seal to the under laying I/O aluminum pad. The solder ball in this structure is connected to silicon base directly. Figure 2 is a schematic view of details of WLP Structure A.

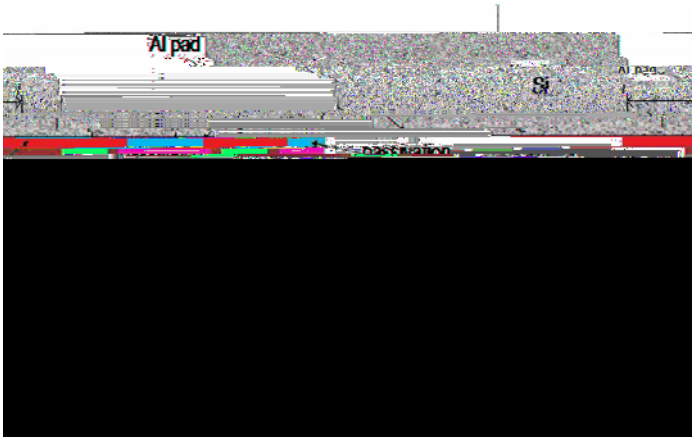


Figure 1 WLP structure A-Standard WLP

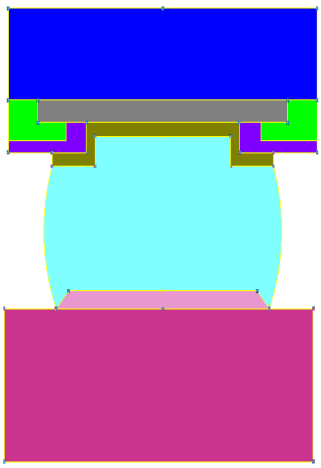


Figure 2 A schematic cross section view of bump structure for WLP Structure A

2.2 WLP Structure B: Ball on Polymer without UBM

Figure 3 shows a schematic diagram of ball on polymer without UBM. Redistribution traces and pads are usually

Figure 5 A schematic diagram of ball on polymer with UBM WLP

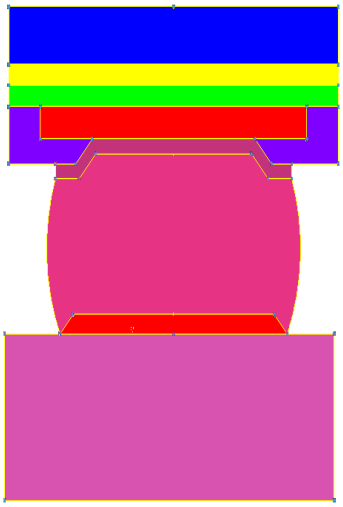
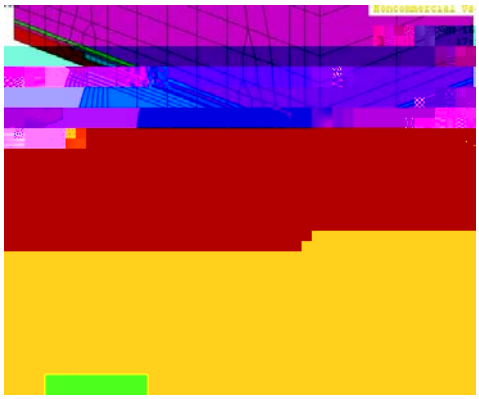


Figure 6 A schematic cross-section view of bump structure for WLP Structure C

2.4 WLP Structure D: Encapsulated Copper Post WLP

In encapsulated copper post WLP technology, bond pads are redirected into an array of interconnects. They are in the form of electroplated copper posts instead of pads to provide enough confrontation for the active wafer surface to be encapsulated in low stress epoxy c 0 Tu atc5v2.7(lat(oxy low)7.s)-5.(p)6at pcd , -1.1453 TD -.0007 Tc .0526 Tw 8

Wafer
Passivation



c)WLP structure C

d)WLP structure D

Figure 11 Finite element models of various WLP structures a). WLP Structure A; b). WLP Structure B; c). WLP Structure C; d). WLP Structure D

Figure 12 Solder bulk crack on package side due to fatigue

3.1 Material Properties

WLP packages are made of different materials. A summary of the materials used for analysis is shown in Table 3. All materials used in the analysis are modeled as linear elastic and the temperature dependency is taken into consideration whenever the glass transition temperature T_g is within the thermal cycling range of -40°C to 125°C. The PCB is fiber reinforced epoxies which makes the properties differ in out of plane direction. Orthotropic properties are therefore used for these materials.

Table 3 Material properties

Materials	Modulas of Elasticity (GPa)	Coefficient of Thermal Expansion

$\hat{s}$, MPa	39.4
n	0.03
D	1.5

3.2 Loading Condition

Stress free initial temperature is important consideration before subjecting any package to loading profile (Fan, 2006) [9]. It is temperature of a material corresponds to the temperature at which the material has either been cured or assembled. There are three commonly used initial stress-free temperature conditions. One is the solidus temperature of solder material (e.g., for SAC305, this temperature is 217°C). This condition considers that the solder joints start to provide mechanical support as soon as the solder material is solidified during the reflow process. The second one is the room temperature as initial stress-free (e.g., 25°C). This assumes that the shipping and storage time is sufficient to relax all the residual stresses in solder joints from the assembly process. The last one uses the high dwell temperature of thermal cycle or operating conditions (denoted as Tmax, e.g. =125°C for thermal cycling from -45°C to 125°C). This assumes that after several thermal cycles, the package reaches a stabilized cyclic pattern where the lowest stresses are seen at the end of the high temperature dwell period.

Figure13 Temperature cycle used for simulation

In this analysis, we have used thermal cycle condition -40°C to 125°C

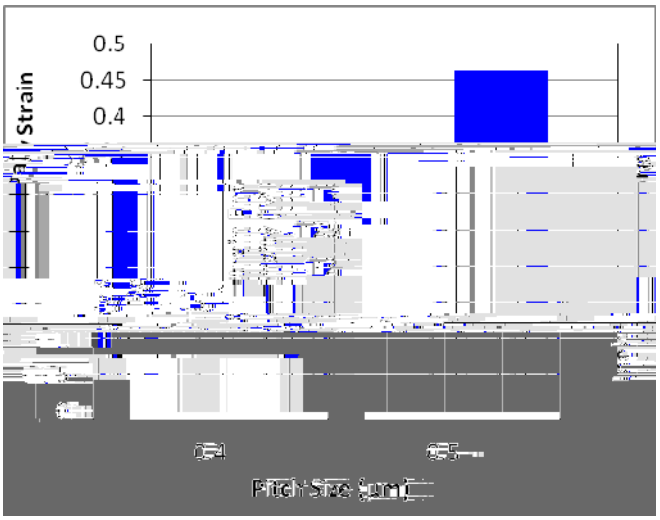


Figure 15 Effect of pitch size

4.2 Effect of Array Size

With increasing array size, inelastic strain energy density continues to increase, therefore fatigue life continues to decreases. Figure 16 shows the results from 6×6 array size to 12×12 array.

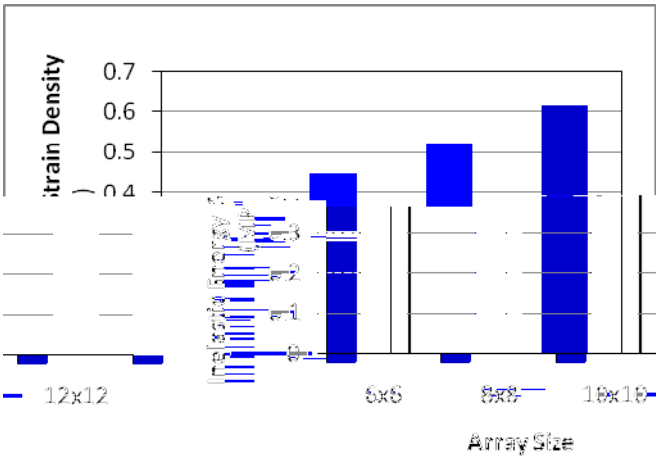


Figure 16 Effect of array size

4.3 Effect of Solder Ball Diameter

By keeping other parameters same, increasing solder ball diameter will increase inelastic strain energy density, and therefore decreases fatigue life under thermal cycling. Figure 17 shows inelastic energy density results for 220µm, 300µm, and 350µm diameters, respectively.

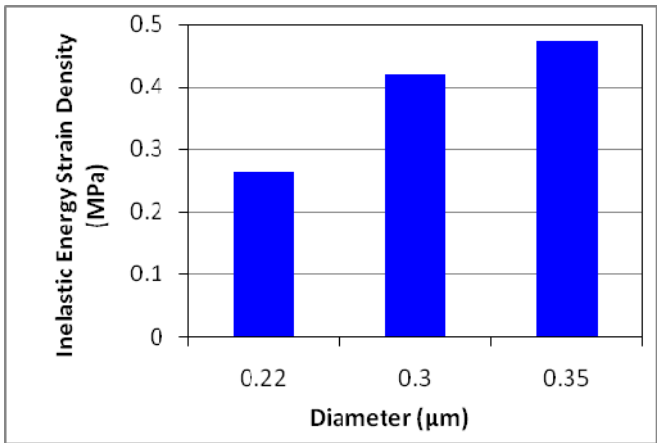


Figure 16 Effect of solder ball diameter

4.4 Effect of Solder Ball Opening Diameter

A larger solder ball opening diameter increases the total contact/interface area, and therefore it takes a longer time for solder ball crack propagations throughout contact interface. Figure 18 shows increasing die size opening diameter from 0.250µm to 0.280µm increases solder joint reliability. It

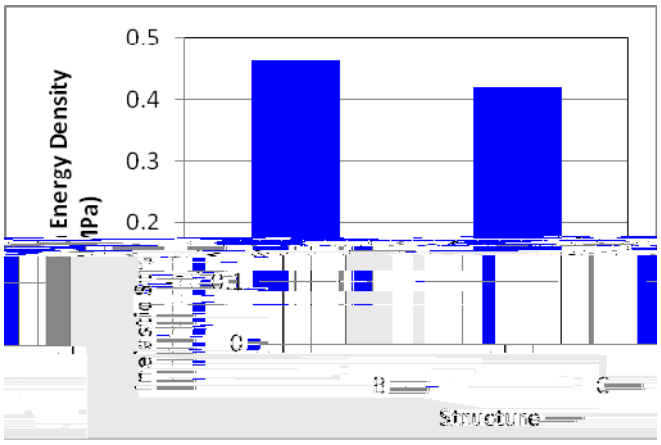


Figure 19 Effect of UBM

4.6 Effect of Passivation Layer

Thermal cycling finite element modeling results show insignificant effect of passivation layer in both structures B and C. Figure 20 shows that eliminating passivation layer in finite element model present good results for both Structure B and C.

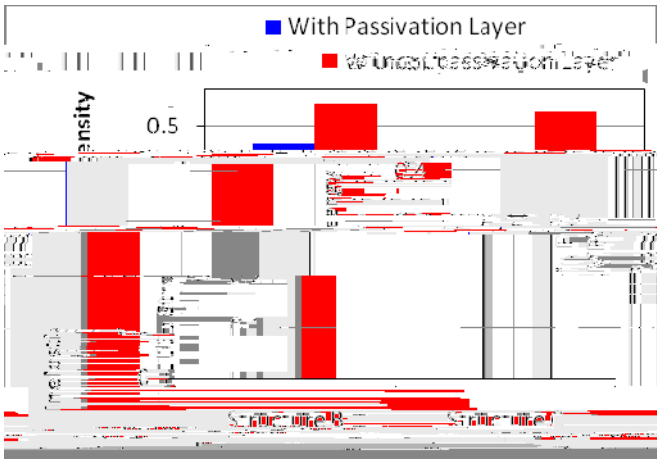


Figure 20 Effect of Passivation Layer

4.7 Effect of Material Properties of Polymer Film 1

Polyimide film is usually used for polymer 1 and 2 in WLP Structures B and C. From Table 3, it can be seen that polyimide is very compliant with a Young's modulus of 1.2GPa, and a coefficient of thermal expansion of 52×10^{-6}/°C respectively. The extreme compliance of polyimide film is often attributed to be the reason for thermal-mechanical performance improvement in solder joints.

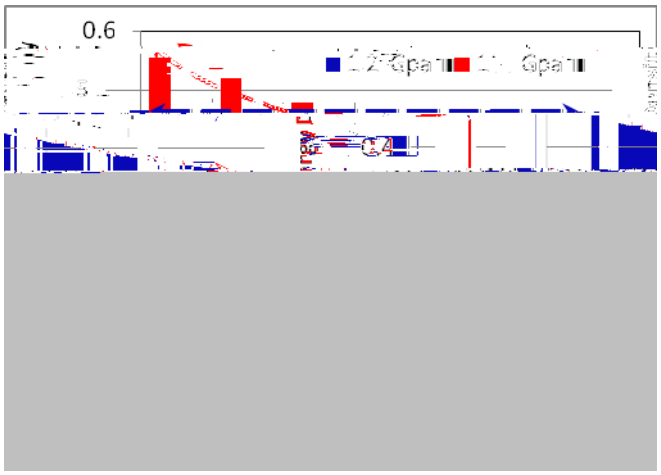


Figure 21 a) Effect of Modulas of Elasticity and CTE of Polymer film in Structure B

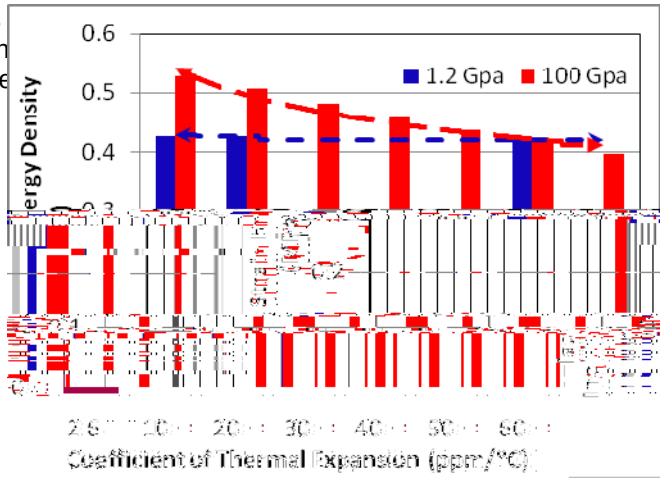


Figure 22 b) Effect of Modulas of Elasticity and CTE of Polymer film in Structure C

A parametric matrix study is performed to understand the effects of Young's modulus and CTE of the film, as shown in Figures 21 (a) and (b), respectively. When the modulus is 1.2GPa, which means that film is extremely compliant, the CTE of the film has no effect on solder joint behavior. However, when film modulus is 100GPa, solder joint stress decreases significantly with the increasing of film CTE. When the CTE is above 50×10^{-6}/°C, solder joint stress is even lower than that the case with the film Young's modulus of 1.2GPa. Such results indicate that the stress buffer effect can be realized either with extreme compliant material or 'hard' material with relatively large CTE. For a very soft film, solder joint stresses are relieved due to large deformation of film. For a hard film with larger CTE, the overall CTE of the combined silicon/film structure increases, therefore, the thermal mismatch with PCB is reduced. Fig. 21 b) show the effects of material properties of polymer film 1 for Structure C, and same conclusion can be reached. Figure 21 c) shows comparison of solder joint reliability of both structures at higher modulas of elasticity of polymer film. It indicates solder joint reliability decreases for UBM

silicon. Lowering the CTE of PCB can also reduce the stresses in solder joints. Figure 25 shows the results of inelastic strain energy density for three set of PCB CTEs. When low CTE PCB core material is used, the fatigue life can be increased greatly. It has been demonstrated that a polymer film layer between solder balls and silicon with a larger CTE can increase the overall effective CTE of silicon, and thus reduce the thermal mismatch with PCB. Similar concept can be developed at PCB side to include a layer of material between PCB and solder balls. The detailed studies will be reported separately.

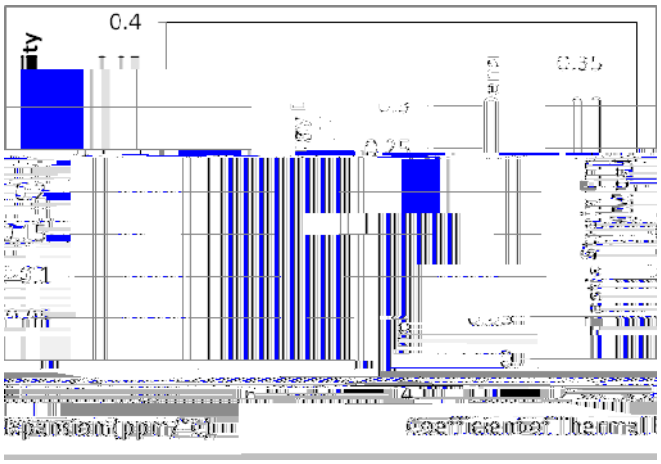


Fig.ure 25 Effect of PCB CTE on solder joint reliability

4.11 Effect of WLP Structure

Fig. 26 shows the per-cycle inelastic strain energy densities for four WLP Structures A, B, C, and D, respectively, for a 12×12 array packages with 0.5mm pitch.

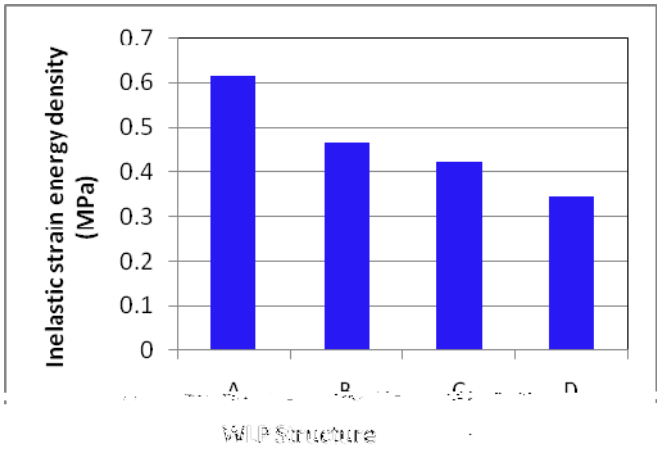


Figure 26 Effect of WLP structure

Compared to the Structure A, all other three Structures B, C and D showed more than 30% reduction in the accumulated inelastic strain energy density per cycle. This means that, with the incorporation of a dielectric polymer film between solder ball and silicon, or an encapsulated copper post layer, the stresses in solder joints can be reduced significantly compared to a 'rigid' connection in Structure A. Structure D with encapsulated copper post showed the best performance. Experimental data have shown that Structure A WLPs can survive only up to 6x6 array size while all other three structures can pass thermal cycling reliability requirement up to 12×12 array sizes (Fan, et al., 2009) [2]. The finite element modeling results are consistent with experimental observations.

4.12 Solder Ball Damage Map

The inelastic energy dissipation plot is given by Figure 27. It is seen that the corner solder ball shows the highest energy dissipation and therefore the largest damage accumulation during temperature cycling. The energy dissipation decays rapidly both along die edge and diagonal direction towards package center. Results show if the corner solder balls are not electrically connected the WLP reliability would be greatly enhanced. This agrees well with the test results.

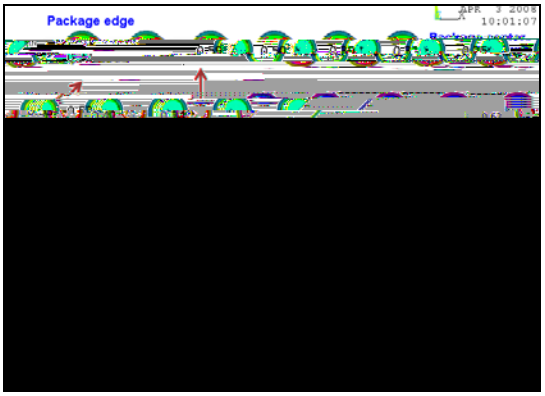


Figure 27 Inelastic Energy Density Contour for Corner Solder Joint

In order to understand the locations of solder joint crack initiation, von Mises stress plot of the solder joints are presented (Figure 28). It is seen that there is stress concentration at both sides for each solder ball. This explains the observation of cracks initiation from both sides of the solder joint. Furthermore, it is seen that the stress is higher at the inner side. This suggests that crack initiates first from inner side. This observation agrees with the findings from the failure analysis.

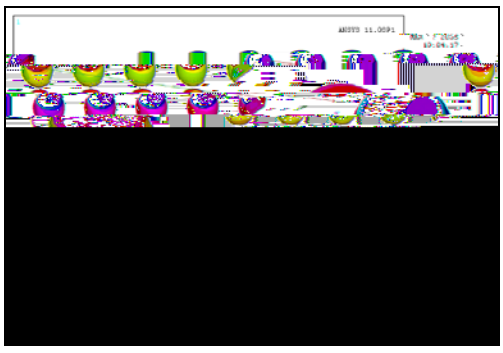


Figure 28 von Mises Stress in Solder Balls for identifying the Critical Ball

5. Experimental Validations [12]

To assess the wafer level package capability and technology limit, the following parameters are considered in experimental study to correlate with simulation results (Rahimet al. 2009) [12].

1. Different WLP structures
2. Ball pitches of 0.5 and 0.4 mm.
3. Array sizes of 12×12 and 10×10

5.1 Array Size

A comparison of failure data for 10×10 and 12×12 array sizes for WLP-C is shown in Table 5. It is observed that WLP-C, 10×10 array has 20% longer fatigue life than 12×12 array. In this case the ratio of WLP size between 12×12 and 10×10 array is 1.2. It appears that the fatigue life is inversely proportional to the package size.

Table 5 Normalized Characteristic Life for 12×12 and 10×10 Array WLP

Array Size	12x12	10x10
Characteristic life	1	1.2

5.2. WLP Ball Pitch

12×12 array WLPs with 0.5 and 0.4mm pitches are tested. WLP fatigue lives are compared against each other (Table 6). It is observed that 0.4mm pitch has 30% longer fatigue life than 0.5mm.

Table 6 Normalized Characteristic Life for 0.5mm and 0.4mm Pitch WLP

Pitch	0.5 mm	0.4 mm
Characteristic Life	1	1.3

Conclusions

Four different WLP structures are studied to investigate the effect of WLP structures on solder joint reliability with a combined modeling, test and failure analysis approach. These four WLP structures are Bump on I/O with and without RDL, Bump on Polymer with UBM, Bump on Polymer without UBM, and Encapsulated Copper Post. Although Ball on I/O WLP structure is limited for the application in small array packages, it has been used as a benchmark here for the analysis. Finite element models for these WLP structures have been created and analyzed. Results showed that Ball on Polymer with and without UBM, as well as Copper Post WLPs had a great improvement in thermo-mechanical reliability performance over the Bump on I/O WLPs.

Thermo-mechanical reliability of solder joints of WLP packages can also be improved by optimizing ball geometry and array size and pitch. The more compliant solder ball is, the greater thermo-mechanical reliability is achieved. Therefore, reducing individual solder ball volume or using more compliant materials such as polymer cored solder balls will improve reliability performance. As solder balls become the weakest link during thermal cycling, increasing the contact area-solder ball opening diameter is the most effective way to improve the solder joint reliability. Also, small array size and lower pitch size has better reliability compare to higher array size and pitch size.

Materials also play important roles in enhancing solder joint reliability. In Ball on Polymer WLP structure, polymer film between silicon and solder balls creates a 'cushion' effect to reduce the stresses in solder joints. Such cushion effect can be achieved either by an extremely compliant film or a 'hard' film with large coefficient of thermal expansion. In the later case, the reduction of solder joint stresses is due to the overall increase of the combined film/wafer effective CTE. It has been found that a 'hard' layer with a large CTE can reduce solder joint stress beyond a compliant film. This has been validated by encapsulated Copper Post WLP structure, which showed the best performance on all four structures in terms of solder joint reliability.

The crack is in bulk solder at package side. The cracks initiate from both sides of the solder joint. The cracksth pac

12. Rahim, M.S.K., Zhou, T., Fan, X.J., Rupp, G. 2009. "Board level temperature cycling study of large array wafer level packages," Proc of Electronic Components and Technology Conference (59th ECTC), pp. 898-902.
13. Syed, A. 2001. "Predicting solder joint reliability for thermal, power, & bend cycle within 25% accuracy," 51st ECTC, pp. 255-263.